REMARKS

Claims 1, 2, 8, 15, 16, and 18-21 have been amended, and new claims 23 and 24 have been added. Thus, claims 1-24 are pending in the present application. The claim amendments and new claims are supported by the specification, claims, and drawings as originally filed, with no new matter being added. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

The specification has been amended to add the patent number of the issued parent application and to provide consistent terminology in the priority claim. Claims 2, 8, 16, 18, and 20-21 have been amended variously to provide consistency in terminology, or to correct typographical errors, and not for reasons related to patentability.

1. Rejections Under 35 U.S.C. § 102

Claims 1-2, 6, 9, 12-13, 15, 17, 19-20, and 22 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,343,354 to Lee et al. (hereinafter "*Lee*") for the reasons set forth on page 2 of the Office Action. Applicants respectfully traverse.

Claim 1 has been amended to recite the "isolation film having an upper surface" and also now recites "forming a gate oxide on said semiconductor substrate such that the gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film." Similar limitations are also now recited in independent claims 15 and 19. Support for these added limitations can be found in the application as filed on page 8, paragraph [023], and in Figures 6 and 7 of the drawings, which show the substantially coplanar relationship of the upper surface of isolation film 20 and the upper surface of gate oxide 22. There is no teaching or suggestion of these recited features in *Lee*.

Lee teaches that a gate insulating layer 1 such as an oxide layer is formed on the upper surface of the semiconductor substrate 100 (col. 5, lines 54-57). As shown in Figure 4B of *Lee*, the gate insulating layer 1 supports a metal electrode 2 at a position above the upper surface of substrate 100. The upper surface of gate insulating layer 1 in *Lee* is not substantially coplanar with the upper surface of isolation region 101, which extends above the upper surface of substrate 100 and gate insulating layer 1 as shown in Figure 4B. While the upper surface of isolation region 101 can be leveled off with the upper surface of substrate 100 (*see* col. 5, lines 30-35), such a configuration would result in the upper surface of gate insulating layer 1 being above the upper surface of isolation region 101.

In contrast, present independent claims 1, 15, and 19 recite that the "gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film." Thus, claims 1, 15, and 19 are not anticipated by *Lee*. Claims 2, 6, 9, and 12-13 depend from claim 1, claim 17 depends from claim 15, and claims 20 and 22 depend from claim 19. Thus, these dependent claims each include the limitations of the respective independent claim, and thus are also not anticipated by *Lee* for at least the same reasons as stated above.

Accordingly, Applicants respectfully request that the rejection of claims 1-2, 6, 9, 12-13, 15, 17, 19-20, and 22 under 35 U.S.C. § 102(b) be withdrawn.

2. Rejections Under 35 U.S.C. § 103

Claims 3, 8, and 18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of *Wolf* (Vol. 2) for the reasons set forth on page 3 of the Office Action. In addition, claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of *Wolf* (Vol. 3) for the reasons set forth on pages 3-4 of the Office Action. Further, claims

10 and 11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of *Wolf* (Vol. 1) for the reasons set forth on page 4 of the Office Action. Applicants respectfully traverse.

Claims 3, 7, 8, 10, and 11 depend from claim 1, and claim 18 depends from claim 15. Thus, these dependent claims each include the limitations of the respective independent claim, including the recitation that the "gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film." As discussed previously, this limitation is not taught or suggested in *Lee*. In addition, such features are also not taught or suggested in *Wolf* (Vol. 1-3). Hence, claims 3, 7, 8, 10, 11, and 18 would not have been obvious over *Lee* in view of *Wolf* (Vol. 1-3).

Applicants therefore respectfully request that the rejection of claims 3, 7, 8, 10, 11, and 18 under 35 U.S.C. § 103(a) be withdrawn.

Claims 4, 5, and 16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of U.S. Patent No. 6,114,216 to Yieh et al. (hereinafter "*Yieh*") for the reasons set forth on pages 4-5 of the Office Action. Applicants respectfully traverse.

Claims 4 and 5 depend from claim 1, and claim 16 depends from claim 15. Thus, these dependent claims each include the limitations of the respective independent claim, including the recitation that the "gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film." As discussed previously, this limitation is not taught or suggested in *Lee*. In addition, such features are also not taught or suggested in *Yieh*. Hence, claims 4, 5, and 16 would not have been obvious over *Lee* in view of *Yieh*.

Applicants therefore respectfully request that the rejection of claims 4, 5, and 16 under 35 U.S.C. § 103(a) be withdrawn.

Claims 14 and 21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* for the reasons set forth on page 5 of the Office Action. Applicants respectfully traverse.

Claim 14 depends from claim 1, and claim 21 depends from claim 19. Thus, these dependent claims each include the limitations of the respective independent claim, including the recitation that the "gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film." As discussed previously, this limitation is not taught or suggested in *Lee*. Hence, claims 14 and 21 would not have been obvious over *Lee* for at least the same reasons as discussed above for claims 1 and 19.

Applicants therefore respectfully request that the rejection of claims 14 and 21 under 35 U.S.C. § 103(a) be withdrawn.

3. New Claims

New independent claim 23 recites similar limitations as present claim 1, and further recites forming a storage node within the container cell, forming a cell dielectric upon the storage node, and forming a cell plate upon the first gate stack, upon the cell dielectric, and upon the second gate stack. These recitations are supported by the application as filed on page 10, paragraphs [029] and [030].

New independent claim 24 recites similar limitations as originally filed claim 1, and further recites forming a storage node, a cell dielectric, and a cell plate as recited in claim 23. Claim 24 further recites that the "cell plate has an upper surface that extends into said container cell." Support for this limitation in claim 24 can be found in Figure 8 of the drawings as filed with the present application. In particular, Figure 8 shows that cell plate 34 is formed such that

its upper surface extends into container cell 28. Such a feature is not taught or suggested in the cited references.

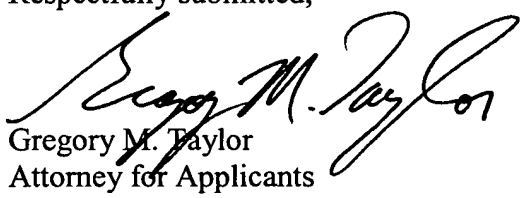
Accordingly, new claims 23 and 24 also present patentable subject matter.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the pending claims. In the event the Examiner finds any impediment to the prompt allowance of this application that could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 31st day of July 2002.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW THE CHANGES MADE

IN THE SPECIFICATION:

Paragraph [01] on page 1 of the specification has been amended as follows:

This application is a continuation of U.S. Patent Application Serial No. 09/249,388, filed on February 12, 1999, now Patent No. US 6,258,660 B1, which is a divisional of [prior application] U.S. Patent Application Serial [Number] No. 08/940,307, filed on September 30, 1997, both of which are incorporated herein by reference.

IN THE CLAIMS:

Claims 1, 2, 8, 15, 16, and 18-21 have been amended as follows:

1. (Once Amended) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate;

forming an isolation film within said trench, said isolation film having an upper surface;

forming a gate oxide on said semiconductor substrate such that the gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks.

2. (Once Amended) A process of forming a container cell as defined in Claim 1, wherein [said] etching a container cell etches said semiconductor substrate such that a portion of said container cell extends beneath said first gate stack.

8. (Once Amended) A process of forming a container cell as defined in Claim 1, wherein etching a container cell comprises [is] an RIE [etch] process.

15. (Once Amended) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate;

forming a conformal isolation film within said trench, said isolation film having an upper surface;

forming a gate oxide on said semiconductor substrate such that the gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks, wherein said semiconductor substrate and said isolation film have an interface that extends below said edge into said semiconductor substrate.

16. (Once Amended) A process of forming a container cell as defined in Claim 15, wherein [said] forming an isolation film is performed by forming an oxide film by the decomposition of TEOS.

18. (Once Amended) A process of forming a container cell as defined in Claim 15, wherein [said] etching a container cell comprises an RIE process.

19. (Once Amended) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate by spinning on a photoresist, masking, exposing and patterning said photoresist to create a photoresist mask, and anisotropically etching through said photoresist mask;

forming a conformal isolation film within said trench by forming an oxide film by deposition, said isolation film having an upper surface;

forming a gate oxide on said semiconductor substrate such that the gate oxide has an upper surface that is substantially coplanar with the upper surface of said isolation film;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks, wherein said semiconductor substrate and said isolation film form an interface that extends below said container cell into said semiconductor substrate.

20. (Once Amended) A process of forming a container cell as defined in Claim [1] 19, wherein said edge and said interface are coplanar.

21. (Once Amended) A process of forming a container cell as defined in Claim [1] 19, wherein said edge and said interface are not coplanar.